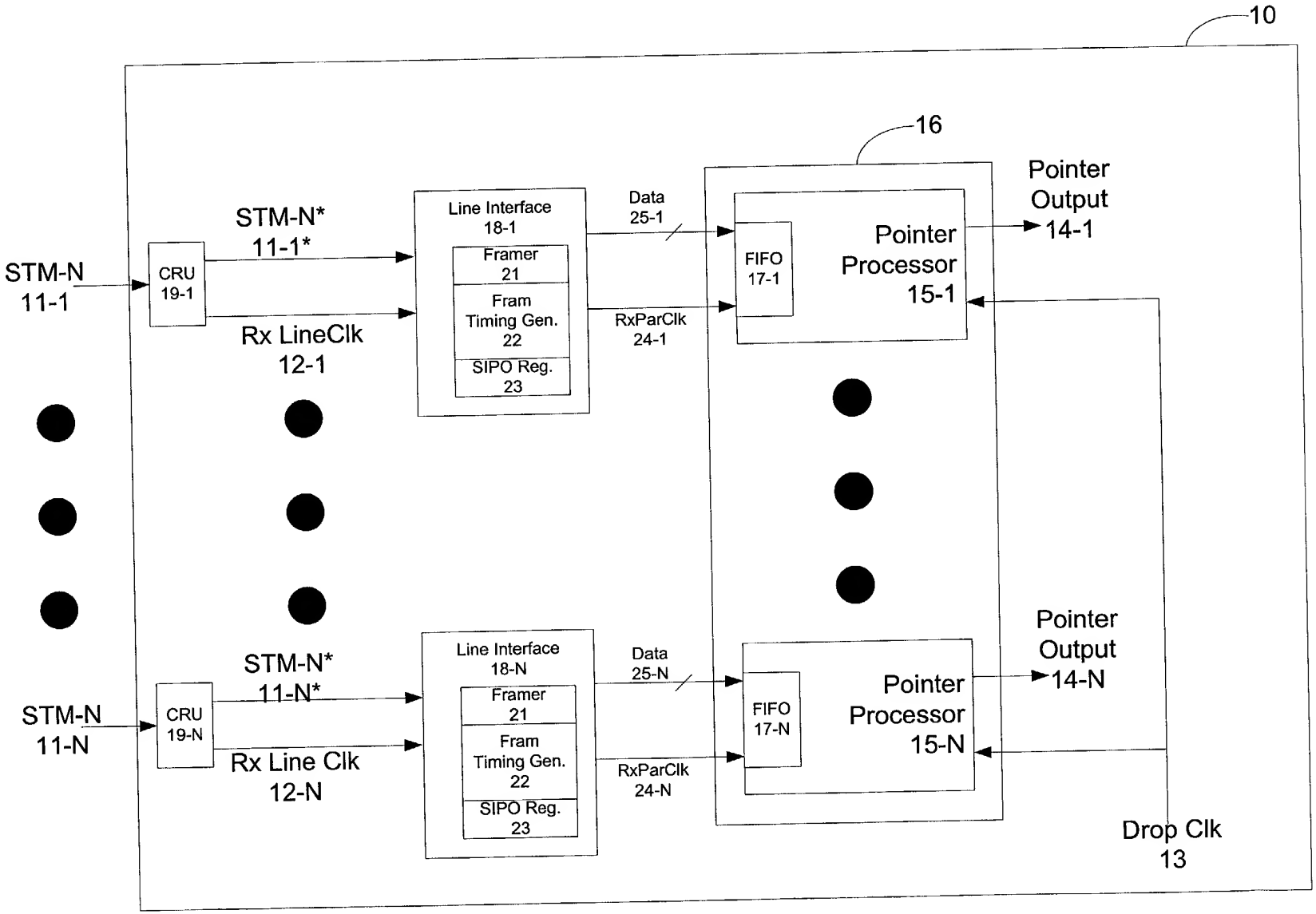

Figure 1 (Prior Art)

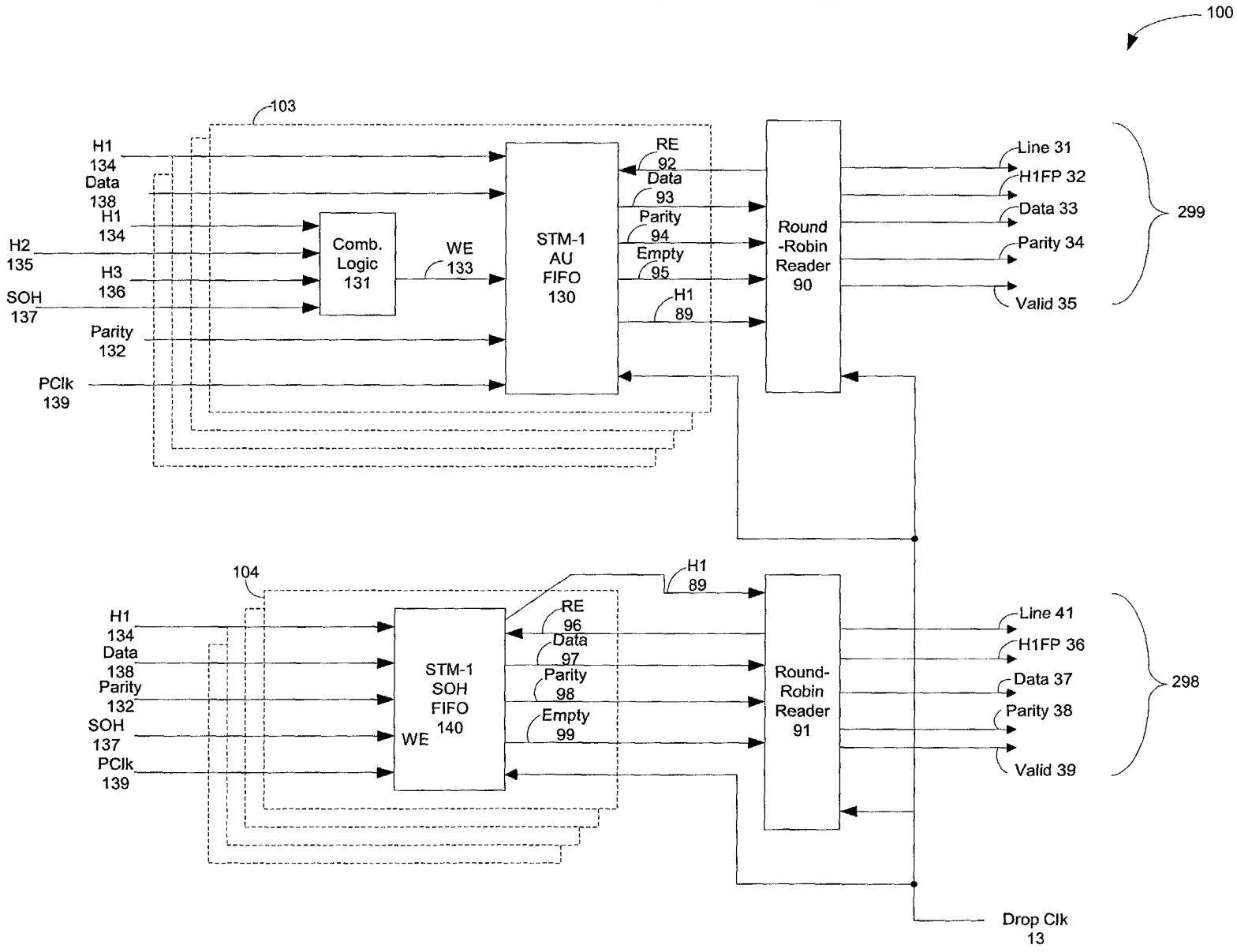
100
103
H1
134
Data
138
H1
134
H2
135
H3
136
SOH
137
Parity
132
PClk
139
Comb.
Logic
131
WE
133
STM-1
AU
FIFO
130
RE
92
Data
93
Parity
94
Empty
95
H1
89
Round
-Robin
Reader
90
Line 31
H1FP 32
Data 33
Parity 34
Valid 35
299
104
H1
134
Data
138
Parity
132
SOH
137
PClk
139
WE
STM-1
SOH
FIFO
140
RE
96
Data
97
Parity
98
Empty
99
H1
89
Round-
Robin
Reader
91
Line 41
H1FP 36
Data 37
Parity 38
Valid 39
298
Drop Clk
13

Figure 2A

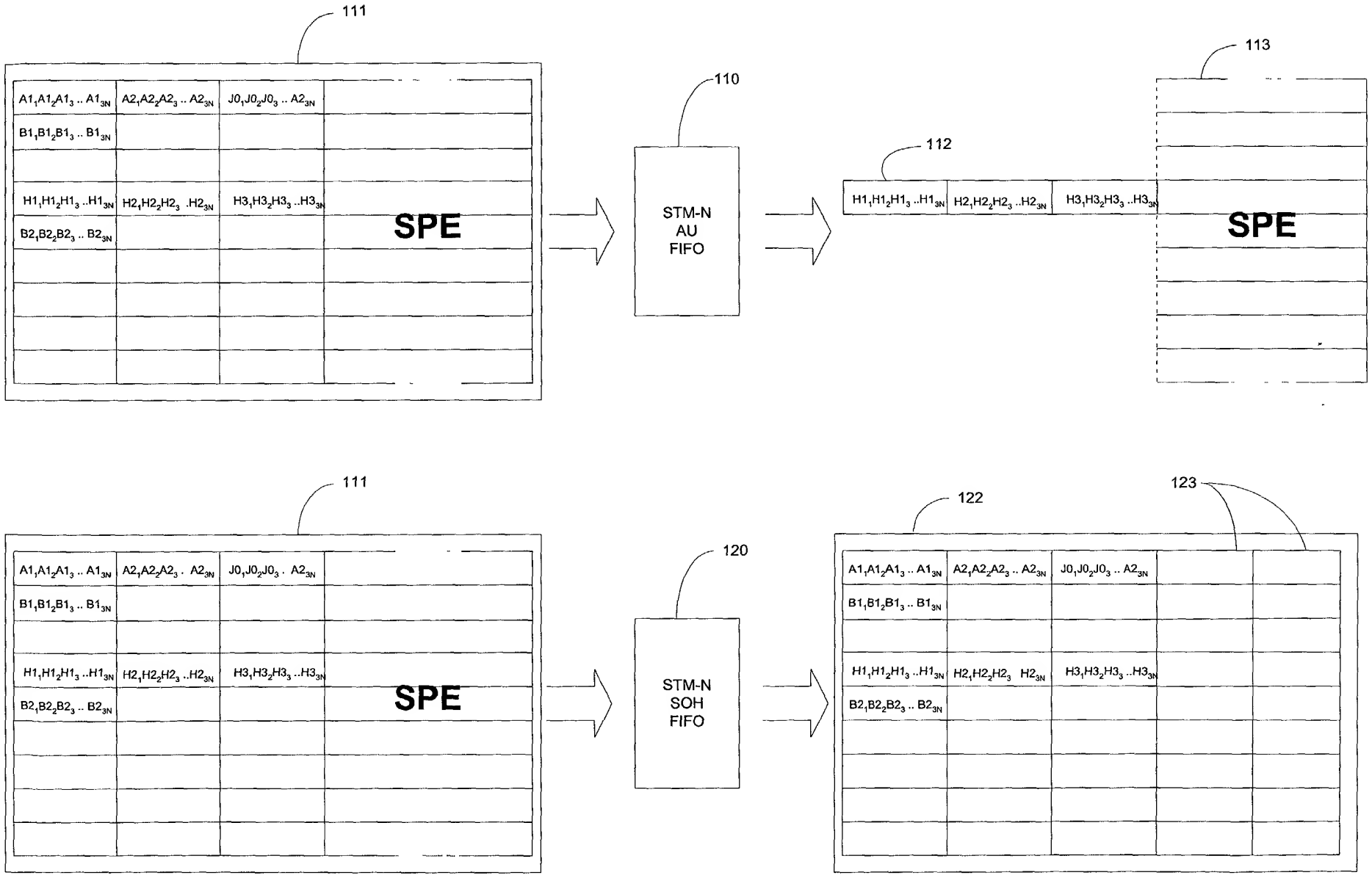

Figure 2B

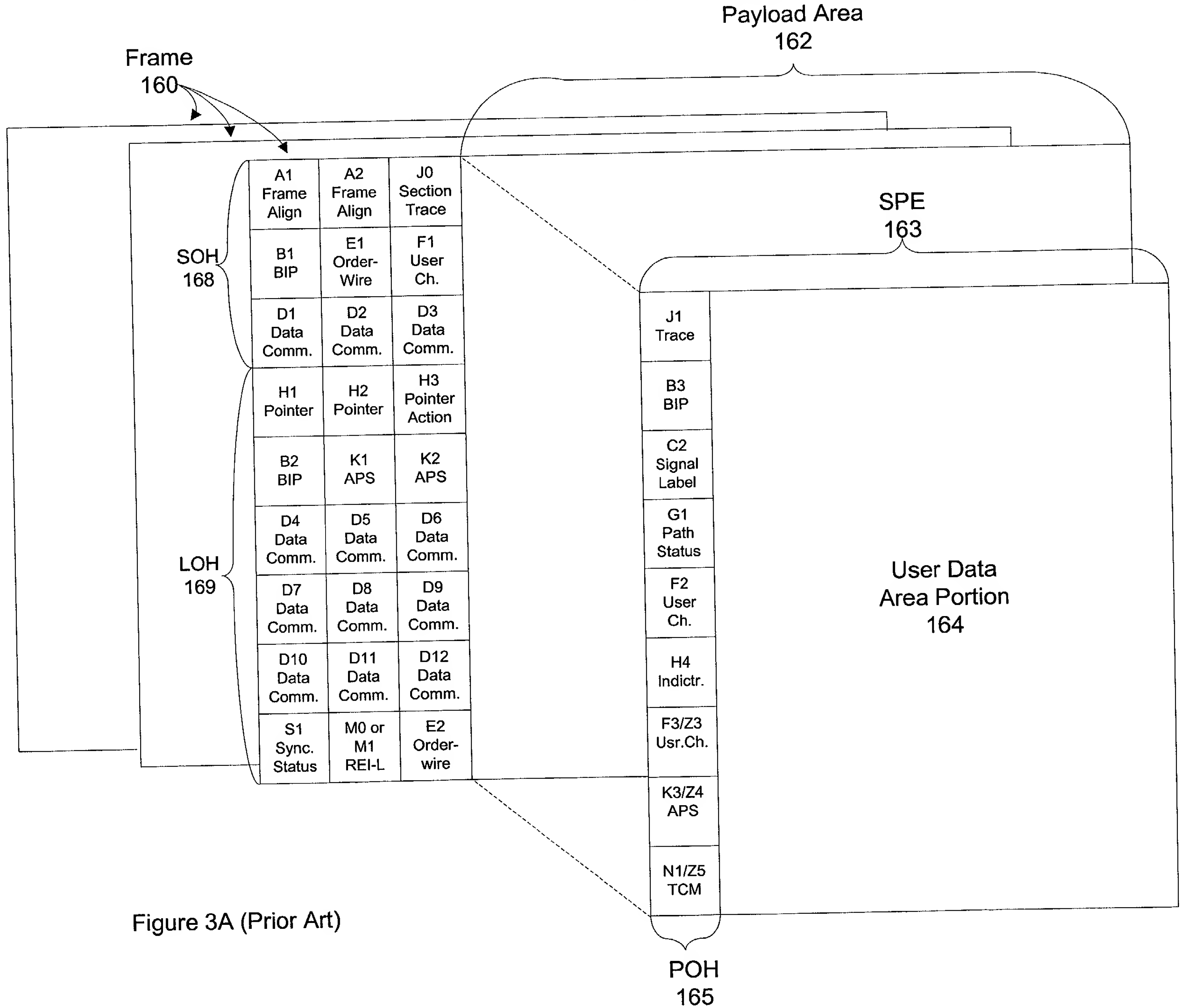

Figure 3A (Prior Art)

Figure 3B (Prior Art)

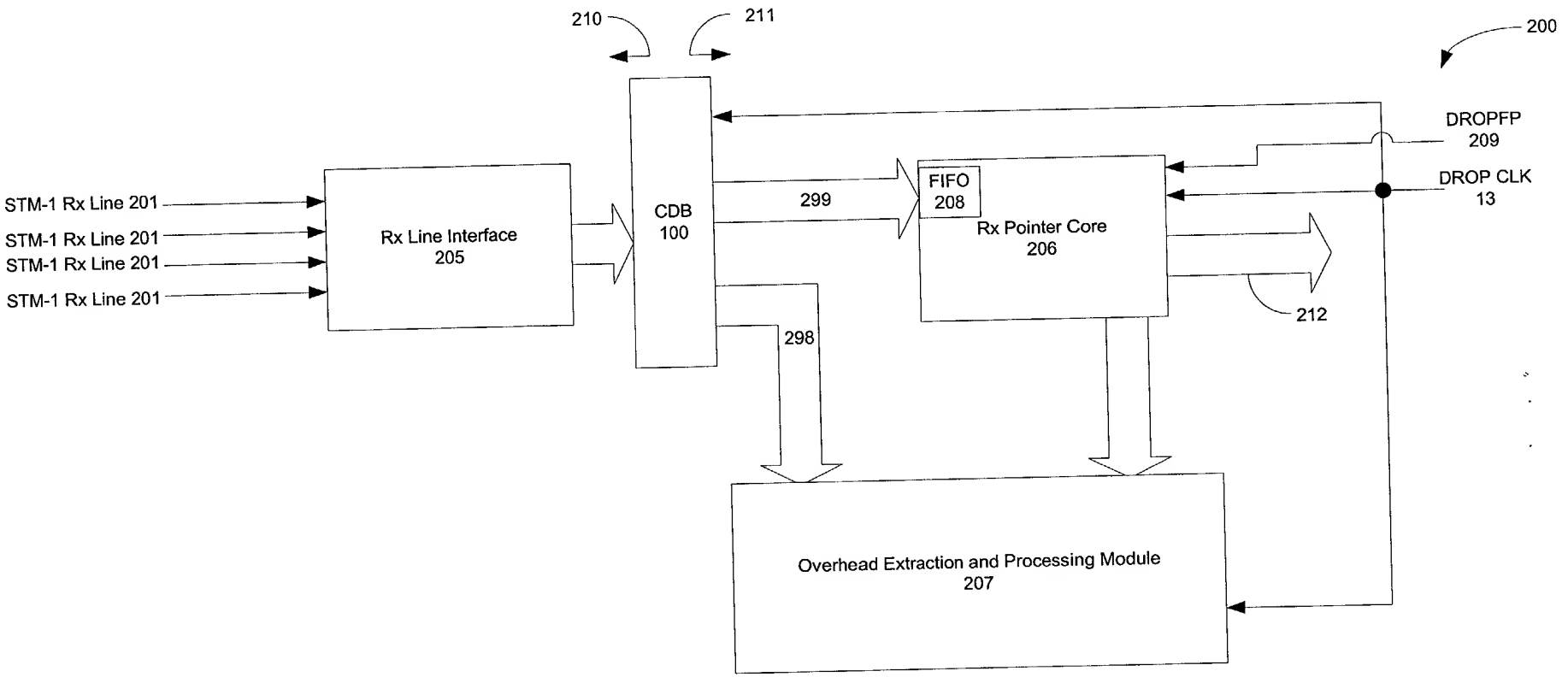
210
211
200
DROPFP
209
DROP CLK
13
STM-1 Rx Line 201
STM-1 Rx Line 201
STM-1 Rx Line 201
STM-1 Rx Line 201
Rx Line Interface
205
CDB
100
299
FIFO
208
Rx Pointer Core
206
212
298
Overhead Extraction and Processing Module
207

Figure 4

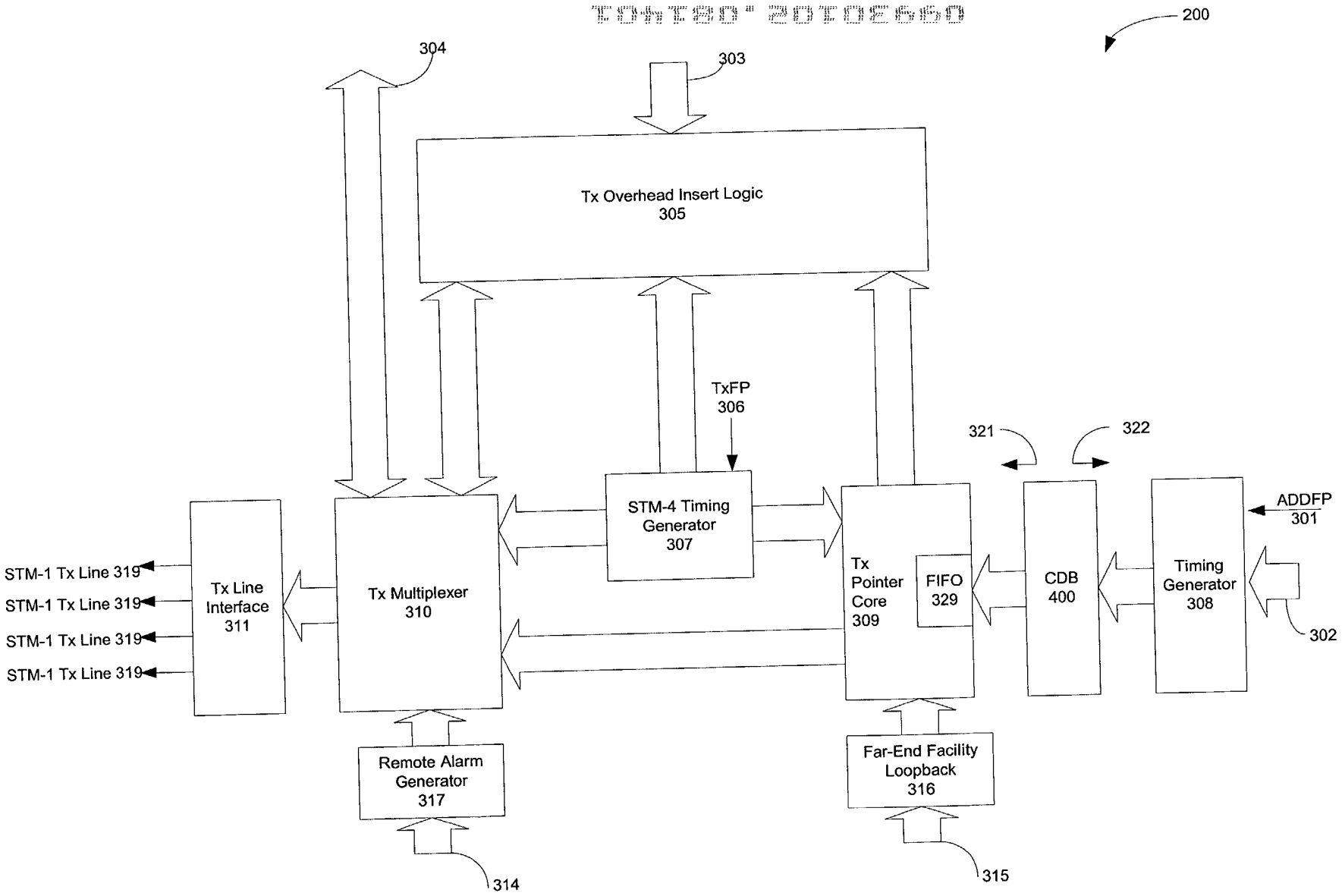
200
304
303
Tx Overhead Insert Logic
305
TxFP
306
321
322
ADDFP
301
STM-4 Timing
Generator
307
Tx
Pointer
Core
309
FIFO
329
CDB
400
Timing
Generator
308
302
STM-1 Tx Line 319
STM-1 Tx Line 319
STM-1 Tx Line 319
STM-1 Tx Line 319
Tx Line
Interface
311
Tx Multiplexer
310
Remote Alarm
Generator
317
Far-End Facility
Loopback
316
314
315

Figure 5

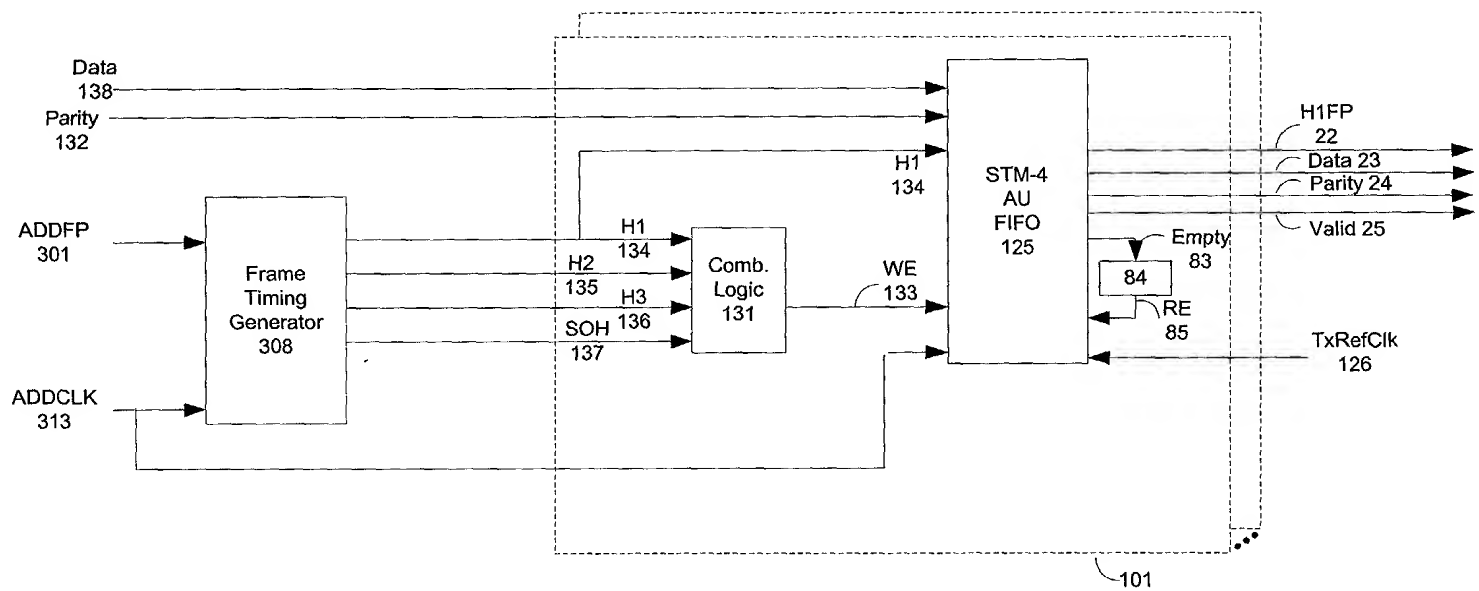
Data
138
Parity
132
ADDFP
301
ADDCLK
313
Frame
Timing
Generator
308
H1
134
H2
135
H3
136
SOH
137
Comb.
Logic
131
WE
133
STM-4
AU
FIFO
125
Empty
83
84
RE
85
H1FP
22
Data 23
Parity 24
Valid 25
TxRefClk
126
101

Figure 6

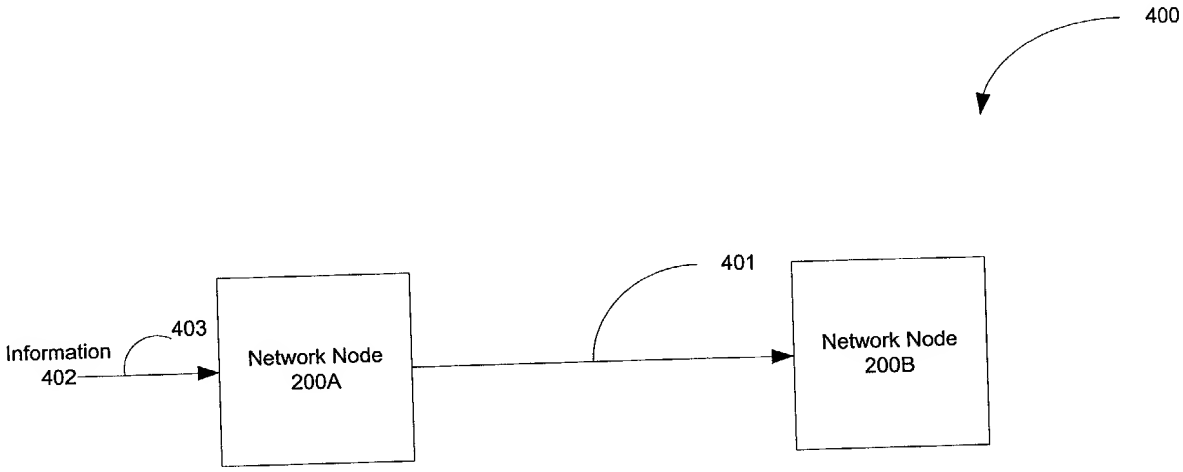
400
401
403
Information
402
Network Node
200A
Network Node
200B

Figure 7